REMARKS

The application has been reviewed in light of the Office Action mailed April 14, 2004. At the time of the Office Action, Claims 1-13 are pending in this application. Claims 1-13 were rejected.

Objection to the Drawings

The drawings are objected to as failing to comply with 37 C.F.R. 1.84(p)(5) because a reference number (303) is not mentioned in the description of the specification. The reference number 303 has been deleted in drawing Figure 3. Applicant respectfully submits a set of replacement drawing Figures 1-4, enclosed herewith, for review by the Examiner and requests that these replacement drawing figures be entered into the file wrapper of the above styled patent application.

Objection to the Title

The title of the invention is objected to as not being descriptive of the invention. The title has been amended as helpfully suggested by the Examiner.

Objection to the Declaration

The Declaration has been objected to as not complying with 37 C.F.R. 1.33(a) by not including the post office address. Applicant has added his post office address to a copy of the originally filed Declaration, and has initialed and dated the changes made thereto. If the Examiner would prefer a Supplemental Declaration to replace the originally filed Declaration as amended, Applicant will comply with any such request.

Objection to the Information Disclosure Statement

The Information Disclosure Statement is objected to because it fails to comply with 37 C.F.R. 1.98(a)(2) which requires a legible copy of each reference cited. Applicant respectfully submits a replacement Information Disclosure Statement form PTO-1449 and legible copies of all references cited therein. The copies of these references are respectfully submitted on a compact disk (CD) in PDF format for convenience of viewing by the Examiner.

Rejection of the Claims under 35 U.S.C. § 102(b)

Claims 1-4 and 9-11 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 3,771,146 to Cotton et al. (hereinafter "Cotton"). Applicant respectfully traverses the rejection and submits that the reference relied upon does not disclose what is being claimed.

The present invention comprises a plurality of registers of which the contents of some or all of the registers may be used as pointers to other memory locations during program execution by a processor. These registers are volatile (do not retain contents during a power loss or brown-out condition). Each of these registers has an associated trap flag that indicates whether the data information is valid or invalid by being in a set or a reset condition, respectively. Valid data is based upon data having been written to the respective register without an intervening power-on or reset event occurring. Trap flag control logic puts each register trap flag into a reset condition upon a power-on or reset occurring. The register trap flag is not put into a set condition until valid data is written to the respective register, and then the pointer registers will be ready for program execution. A trap interrupt is only generated when a processor program instruction tries to use the contents of a register as an address pointer to another memory location and the associated register trap flag is in the reset condition. The

invention insures that only those registers having valid data (address information) are used during program execution. Thus, there can be no program addressing errors caused by a power-up or reset condition occurring during execution of a program by a processor.

In contrast to the present invention, Cotton discloses a multiprocessor computer system having capability registers arranged to store a capability word that is used to indicate address ranges for particular memory segments in the multiprocessor computer system. The capability register for each memory segment stores a capability word relating to the particular memory segment to which a processor requires access in the performance of the current process. A purpose of the Cotton invention is to enable a plurality of processors to utilize common memory by segmenting the memory for each processes being performed by each of the plurality of processors. The Cotton invention may force entry into an interrupt handler process (routine) when a capability register is loaded with a discrete code (*i.e.*, all zeros). The discrete code in a capability register may be used (1) to prevent access to a memory segment by all applications programs typically when that memory segment is being relocated within main memory or being up-dated; (2) cause an interrupt to an interrupt program for dealing with a system resource; and (3) to prevent a particular processor from accessing a particular memory segment. Col. 1, line 60 to col. 2. line 33; col. 5, lines 17-59; and col. 17, lines 26-42.

Cotton does not disclose causing trap flags associated with volatile memory registers to be in a reset condition when a processor power-up or reset occurs, nor does Cotton disclose causing a trap flag to be placed in a set condition when an associated memory register has valid data written therein. Thus, the present invention is directed to preventing program operation errors do to volatile memory register corruption, and to only allow a trap flag to in a set condition when know valid data has been written thereto, as recited in independent claims 1

and 9. Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention arranged as in the claims.

Claims 2-4 depend from independent claim 1 and claims 10 and 11 depend from independent claim 9, and contain all limitations thereof.

Rejection of the Claims under 35 U.S.C. § 103(a)

Claims 5-8, 12 and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cotton in view of U.S. Patent No. 3,886,524 to Darren R. Appelt (hereinafter "Appelt"). Claim 5 has been canceled. Applicant respectfully traverses the rejections and submits that the references relied upon do not teach or suggest, individually or in combination, what is being claimed.

Cotton does not teach or suggest preventing program operation if an address pointer register may not have valid address data therein. As discussed above, the present invention always forces trap flags to be in a reset condition when a processor power-up or reset occurs. Only when each individual register that is used as a program address pointer has valid data written to it, will the associated trap flag be in a set condition. Otherwise, use of a register for program address pointing without the corresponding trap flag being in the set condition, will cause a program exception or trap so that the pointer registers will have valid data written therein. Cotton teaches protecting memory segments from undesired processes and processors. Three is no suggestion of in Cotton of preventing use of volatile registers for address pointers if the data in the pointer registers is not valid by specifically writing the data to the register, nor does Cotton suggest causing all trap flags associated with volatile registers to be placed into a reset condition when a power-up or reset is detected. Normally a power-up or reset results in volatile memory registers containing invalid data. Cotton teaches memory segment sharing

protection between a plurality of processor and processes, not prevention of improper operation of a program due to program address pointer registers having invalid data due to a processor system power-up or reset.

Appelt teaches an asynchronous bus for communication among master and slave computer devices. The reset signal relied upon as a prior art rejection (col. 9, lines 30-48) taught in Appelt is a common type of reset signal that forces all sequential logic to predefined logic levels. However, Appelt does not teach or suggest causing a specific trap flag to be in a set condition when its associated pointer register is written to with valid data program address information. In addition, Appelt does not teach or suggest checking a trap flag (bit) before using the data contained in an associated pointer register for program address information.

According to the present invention, all trap flags are put into a reset condition upon the detection of a processor power-up or reset, and only those trap flags associated with pointer registers will be put into a set condition if the associated pointer register has valid data written thereto. Then the data contained in the pointer register will only be used as a program address if the associated trap flag is in a set condition, otherwise, a trap handling routine may be initiated, and the program will not use the invalid data as a program address.

Applicants respectfully submit that the references relied upon do not teach or suggest, individually or in combination, that all trap flags are put into a reset condition upon the detection of a processor power-up or reset, and only those trap flags associated with pointer registers will be put into a set condition if the associated pointer register has valid data written thereto. Then the data contained in the pointer register will only be used as a program address if the associated trap flag is in a set condition, otherwise, a trap handling routine may be initiated, and the program will not use the invalid data as a program address.

Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. In addition, the suggested combination could not be achieved without significant structural modification of either reference since there is no teachings or suggestion to individually put a trap flag into a set condition only if an associated pointer register has valid data written thereto, nor do these references suggest checking the trap flag to be in a set condition before using the pointer register for program addressing.

Many electronic digital systems use a reset to either hold circuits to a predefined condition and/or force sequential circuits to known or predefined states. However, the references relied upon do not teach or suggest, individually or in combination, relying upon a set condition being present in a trap flag associated with a specific pointer register before using the data contained in the pointer register as a program address, nor do the references relied upon teach or suggest that the trap flag will only be in a set condition if valid data has been written to the associated pointer register after the occurrence of any power-up or reset. If an attempt is made by a program to use invalid data (trap flag in a reset condition) from a pointer register as a program address, the present invention may cause a trap routine to occur, thus, having the capability of replacing the invalid data that may be in the pointer register with valid data, and by doing so, put the associated trap flag into a set condition so that the program may now utilized this known valid data in the pointer register as a valid program address.

Claims 6-8 depend from independent claim 1, and claims 12 and 13 depend from independent claim 9, and contain all limitations thereof.

All amendments are made in a good faith effort to advance the prosecution on the merits. Applicant reserves the right to subsequently take up prosecution on the claims as

originally filed in this or appropriate continuation, continuation-in-part and/or divisional applications.

Applicant respectfully requests that the amendments submitted herein be entered, and further requests reconsideration in light of the amendments and remarks contained herein.

Applicant respectfully requests withdrawal of all objections and rejections, and that there be an early notice of allowance.

SUMMARY

In light of the above amendments and remarks Applicant respectfully submits that the application is now in condition for allowance and early notice of the same is earnestly solicited. Should the Examiner have any questions, comments or suggestions in furtherance of the prosecution of this application, the Examiner is invited to contact the attorney of record by telephone or facsimile.

Applicant believes that there are no fees due in association with the filing of this Response. However, should the Commissioner deem that any fees are due, including any fees for extensions of time, Applicant respectfully requests that the Commissioner accept this as a Petition Therefor, and direct that any and all fees due are charged to Baker Botts L.L.P. **Deposit Account No. 02-0383**, *(formerly Baker & Botts, L.L.P.)* **Order Number 068354.1445**.

Respectfully submitted,
BAKER BOTTS L.L.P. (023640)

By: Paul M. Katz

Paul N. Katz
Reg. No. 35,917
One Shell Plaza
910 Louisiana Street
Houston, Texas 77002-4995
Telephone: 713.229.1343
Facsimile: 713.229.7743
E-Mail: Paul.Katz@bakerbotts.com
ATTORNEY FOR APPLICANT

July 19, 2004